

Call for Papers

— *Special Section on Multiple-Valued Logic and VLSI Computing* —

Recent development of System-on-Chip (SoC) technology has been accelerated by device scaling which drives improved performance and power, high functionality and cost reduction. However, there occur unprecedented serious problems today at very small device feature sizes. To solve the problems, innovative new-concept VLSI computing technology such as multiple-valued VLSI computing is strongly expected to be developed. Also, logic design based on a multiple-valued concept, multiple-valued algebra and soft computing are expected to be effectively employed for the next-generation digital computing and artificial intelligent applications. From this point of view, we have planned Special Section on Multiple-Valued Logic and VLSI Computing to be published in August, 2010. To discuss the same frontier area, the 39th IEEE International Symposium on Multiple-Valued Logic (ISMVL'09) was held in May 21-23, 2009 in Okinawa, Japan. We solicit for submission of the papers on multiple-valued logic and VLSI computing, not limited to the presented papers in the ISMVL'09. We welcome demonstration of the recent development of novel and new-concept computing technology,

Topics of interest include, but are not limited to:

Multiple-Valued Algebra and Logic, Fuzzy Logic, Soft Computing, Quantum Computing, Multiple-Valued Logic Design and Switching Theory, Test and Verification, Spectrum Technique, New-Concept VLSI Architecture, Multiple-Valued VLSI Computing, Nanodevice-Based Architecture, etc.

Guideline for paper submission:

The deadline for submission is **November 10, 2009**. The length is recommended within 8 printed pages for a paper. Manuscript should be prepared according to the guideline in the "Information for Authors". The latest version is available at the web site, http://www.ieice.org/eng/shiori/mokuji_iss.html. The term for revising the manuscript after acknowledgement of conditional acceptance for this special section could be shorter than that for regular issues (60 days) because of the tight review schedule.

This special section will accept only papers by electronic submission. Prospective authors are requested to follow carefully the submission process described below.

1. Submit a paper using the IEICE Web site https://review.ieice.org/regist_e.aspx. Authors should choose the "[Special-ED] Multiple-Valued Logic and VLSI Computing" as a "Type of Issue (Section)/Transactions" on the online screen. Do not choose "[Regular-ED] Information and Systems" or other special sections.
2. Send "Copyright Transfer and Page Charge Agreement" and "Confirmation Sheet of Manuscript Registration" to the following contact person by postal mail. (NOT by FAX or E-mail) **until November 10, 2009**. There is a possibility that we shall withdraw the manuscript without receiving them, even if we have received the manuscript.

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* Please note that if accepted, all authors are requested to pay for the page charges covering partial cost of publications.

*At least one of the authors must be an IEICE member when the manuscript is submitted for review. We recommend that authors unaffiliated with IEICE apply for membership. For membership applications, please visit the web-page, <http://www.ieice.org/eng/member/OM-appli.html>