39th IEEE International Symposium on Multiple-Valued Logic

Naha, Okinawa, Japan

May 21-23, 2009

CALL FOR PAPERS

The Multiple-Valued Logic Technical Committee of the IEEE Computer Society will hold its 39th annual symposium on May 21-23, 2009 in Naha, Okinawa, Japan.
The event is sponsored by the IEEE Computer Society and Japan MVL Research Group.
You are invited to submit an original paper, survey or tutorial paper on any subject in the area of multiple-valued logic, including but not limited to:

Algebra and Formal Aspects,
Automatic Reasoning,
Logic Programming,
Philosophical Aspects,
Fuzzy Logic and Soft Computing,
Data Mining,
Machine Learning and Robotics,
Quantum Computing,
Logic Design and Switching Theory,
Test and Verification,
Spectral Techniques,
Circuit/Device Implementation,
VLSI Architecture,
VLSI Computing,
System-on-Chip Technology,
Nano Technology

Authors should submit papers by **November 1, 2008** to:
Prof. Takahiro Hanyu, Program Chair
Research Institute of Electrical Communication, Tohoku University,
2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan
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Electronic submissions by PDF or PS files are strongly preferred. In exceptional cases, submissions of four (double-spaced typed) paper copies are also acceptable. Each manuscript should include a 50-100 word abstract should not exceed 6 pages in the proceedings format.

Authors will be notified about acceptance by **February 1, 2009**.
Photo-ready copies of accepted papers are due on **March 1, 2009**.
For submission details, visit : http://cs3.el.gunma-u.ac.jp/ISMVL2009

For additional information contact:
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The symposium will be preceded by the Post Binary ULSI Workshop on May 20, 2009.